REMARKS

Claims 1-21 were originally presented for examination. Claims 4-9 are 11-21 are in original form. Claims 22-38 have been added by way of the present Response.

Claims 1-38 are currently pending, of which claims 1, 10, 16, 22, 29, and 34 are in independent form. Favorable reconsideration of the present Response as currently constituted is respectfully requested.

Applicant gratefully appreciates the indication of allowable subject matter. In the outstanding Office Action, the Examiner has indicated that claims 4-7, 15, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant has presented the allowable subject matter of claim 4 in new claim 22, of claim 15 in new claim 29, and of claim 21 in claim 34. Accordingly, Applicant respectfully submits that claims 22, 29, and 34 are allowable. Additionally, claims 23-28, which depend from claim 22 and add further limitations therein; claims 30-33, which depend from claim 29 and add further limitations therein; and claims 35-38, which depend from claim 34 and add further limitations therein, are also in condition for allowance.

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DOCKET NO.: 10010394-1

Regarding the Claim Rejections - 35 U.S.C. §102(e)

In the pending Office Action, claims 1-3 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,279,119 to Bissett et al. (hereinafter the *Bissett* reference). The Examiner provided the following comments with respect to these §102 rejections:

> Regarding claim 1:
> a. Regarding the limitation of "providing a synchronous breakpoint at a predetermined address location with respect to said code portion," Bissett discloses a system with an interrupt that can be performed after a fixed amount of clock cycles. (Lines 43-45 of Column 3). Bissett also disclose that a breakpoint may be generated after a fixed number of instructions. (Lines 45-47 of Column 3).
> b. Regarding the limitation of "executing said code portion on said processors in said simulated multiprocessor environment from a fixed location," Bissett discloses a system wherein computed elements can be configured to refresh operation to synchronize execution of operation. (Lines 26-30 of Column 3).
> c. Regarding the limitation of "when a first processor of said processors encounters said synchronous breakpoint, terminating execution of said code portion on said first processor while continuing to execute said code portion on remaining processors," Bissett discloses a system wherein processing can be aligned by the interrupts. (Lines 53-59 of Column 3). Bissett discloses that interrupts maybe generated after a fixed number of instructions. (Lines 45-47 of Column 3).

The present invention, as defined by independent claim 1, is directed to a scheme of synchronizing processors in a simulated multiprocessor environment operable to execute a code portion to be debugged. In particular, a synchronous breakpoint is utilized that terminates execution of the code portion on a first processor while the execution of the code portion continues on the remaining processors. Applicant respectfully submits that the *Bissett* reference neither discloses nor suggests the present invention as defined by independent claim 1.

The *Bissett* reference is directed to a fault resilient/fault tolerant computer system that includes at least two compute elements connected to at least one controller. The compute elements operate in a first mode in which the compute elements each execute a first stream of instructions in an emulated clock lockstep. The compute elements also operate in a second mode in which the compute elements each execute a second stream of instructions in an instruction lockstep. Please see the *Bissett* reference, column 2, 60 - column 3, line 9. The compute elements transition from the first mode of operation to the second mode of operation in response to an interrupt. Please see the *Bissett* reference, column 3, lines 40-42.

Applicant respectfully submits that the Examiner has mischaracterized the interrupt of the *Bissett* reference as teaching the claimed synchronous breakpoint which terminates the execution of a code portion on a first processor while continuing the execution of the code portion on the remaining processors. The interrupt of the *Bissett* reference transitions the compute elements between a first mode, wherein a first set of instructions are performed in clock lockstep, and a second mode, wherein a second set of instructions are performed in instruction lockstep. Hence, contrary to Applicant's recited claims and the Examiner's characterization, the interrupt of the *Bissett* reference does not terminate the code execution on one of the compute elements while continuing the code execution on the other compute element. Rather, the interrupt of the *Bissett* reference terminates the clock lockstep execution of a first set of instructions on both compute elements and initiates the instruction lockstep execution of a second set of instructions on both compute elements.

Accordingly, Applicant respectfully submits that the *Bissett* reference neither discloses nor suggests Applicant's invention as recited in claim 1. Dependent claims 2-9 depend from this base claim and introduce additional limitations therein. Accordingly,

dependent claims 2-9 of the present patent application are also allowable.

Regarding the Claim Rejections - 35 U.S.C. §103(a)

In the pending Office Action, claims 10-14 and 16-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,694,449 to Ghameshlu et al. (hereinafter the *Ghameshlu* reference) in view of the *Bissett* reference. Also, claims 8 and 9 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Bissett* reference as applied to claim 1 above, and further in view of the *Ghameshlu* reference. The following comments were provided by the Examiner with respect to these §103 rejections:

> Regarding claim 10:
> d. Regarding the limitation of "providing an architectural simulator operable to simulate said target hardware platform, said architectural simulator having a debugger associated therewith, wherein said target hardware platform comprises a multiprocessor system," Ghameshlu discloses a system with a multiprocessor environment (Lines 15-17 of Column 8), with an error diagnosis in the processor.
> e. Regarding the limitation of "initializing in said architectural simulator a list of processors included in said target hardware platform," Ghameshlu discloses a system with a multiple processor devices and Ghameshlu discloses a crossover bus connects at least one further processor device to the first process, in which signature data is passed over the bus. Ghameshlu

does not disclose a system with a list of processors in the target hardware. Bissett discloses a multiple processor system that stores a configuration list of processors operating normally. (Lines 65-67 of Column 6). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the art of Ghameshlu and Bissett. One of ordinary skill would have been inclined to combine the art because Ghameshlu discloses a need for a way to store signature information received over the crossover bus wherein the signature passed over the passed in check with a stored signature for error handling. (Lines 60-67 of Column 3 and Lines 1-4 of Column 4). Bissett disclose a system in which a configuration list is maintained for the transmission of the state information of the processor. (Lines 65-67 of Column 6 and Lines 1-2 of Column 7).

f. Regarding the limitation of "setting a synchronous breakpoint at a predetermined address location with respect to said code portion operable to be executed on said architectural simulator," Bissett discloses a system with an interrupt that can be performed after a fixed amount of clock cycles. (Lines 43-46 of Column 3).

g. Regarding the limitation of "launching said code portion on said architectural simulator from a fixed location," Ghameshlu discloses a system with a comparer to receive data and launches an error handling program. (Lines 18-20 of Column 4).

h. Regarding the limitation of "automatically stepping through said list of processors until each of said processors of said architectural simulator reaches said synchronous breakpoint," Ghameshlu discloses a system with the ability to continue operation in the processor system on the remaining processor to achieve a frictionless continuation of the operations being processed. (Lines 25-33 of Column 6).

i. Regarding the limitation of "returning program control to said debugger for performing a debug operation," Ghameshlu discloses a system with an

error diagnosis that triggers error handling. (Lines 20-22 of Column 4).

Similar comments were also provided by the Examiner with respect to the base claim 16. The present invention, as defined by independent claims 10 and 16, is directed to a scheme for debugging a code portion targeted for execution on a target hardware platform. In particular, a list of processors is stepped through until each of the processors reaches a synchronous breakpoint. Applicant respectfully submits that the combination of the *Bissett* and *Ghameshlu* references does not suggest the present invention as defined by the independent claims.

As discussed in detail hereinabove, the *Bissett* reference neither discloses nor suggests the claimed synchronous breakpoint as recited by Applicant. The *Ghameshlu* reference does not cure the deficiencies of the *Bissett* reference as applied against the claimed invention. The *Ghameshlu* reference discloses a duplicable processor device that, with reference to Figure 1, includes a processor controller PSR having two processor devices MPU and MPU'. In the event of an error or the need for service, the operations being performed on the MPU may be switched over to the MPU' in order to provide duplication or redundancy. Please see the

Ghameshlu reference, column 6, lines 24-33 and column 7, lines 11-38. The *Ghameshlu* reference is concerned with redundant computer architectures and does not disclose or even tangentially discuss debugging code. Hence, the *Ghameshlu* reference does not contain any suggestion or motivation for providing a synchronous breakpoint that is utilized to debug a code portion targeted for a target hardware platform.

Accordingly, Applicant respectfully submits that the combination of the *Bissett* and *Ghameshlu* references does not suggest Applicant's invention as recited in claims 10 and 16. Dependent claims 11-14 and 17-20 depend from these base claims and introduce additional limitation therein. Accordingly, dependent claims 11-14 and 17-20 of the present patent application are also allowable. Further, in view of the foregoing remarks, claims 8-9 are allowable as these claims depend from claim 1 and add further limitations.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the present invention, as now defined by the independent claims, and in further view of the above amendments and remarks, reconsideration of the Action and allowance of the present invention are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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